A 900 MHz Low Phase Noise CMOS Quadrature Oscillator

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Abstract **— A novel method for designing quadrature oscillators is presented. The technique is based on differential coupling at the second harmonic frequency of two separate oscillators. The desired coupling is obtained using an integrated transformer which is attached to the common-mode nodes of two differential oscillators. A 900 MHz prototype has been implemented in a 0.35 μm CMOS process. The oscillator core consumes 3 mA of current from a 1.7 V DC supply and results in an output power of –9 dBm per oscillator, and a measured phase noise of –116, -133 and –138 dBc/Hz at 100 KHz, 600 KHz and 1 MHz from the carrier, respectively. The proposed method is ideal for oscillators operating at 2.5 GHz, 3.5 GHz and 5 GHz.**

I. Introduction

Quadrature oscillators are a key component in direct-conversion transceivers. These oscillators play a fundamental role in image-rejection techniques based on the proper phasing of the signals. They also remove the bulky and non-planar high-frequency filters. Moreover, some digital radio communication systems (e.g. GSM and DECT), where complex digital modulation schemes are used in order to minimize the signal bandwidth, require quadrature oscillators [1]. In these applications, departures from the quadrature phase or the presence of an amplitude imbalance between the two signals result in a detrimental effect on the overall system performance.

Different implementations of quadrature oscillators can be found in the literature:

1) A standard VCO followed by a RC-CR phase-shift network. Inaccuracies in the actual values of R and C can lead to errors in the quadrature and require some form of compensation [2].
2) A VCO running at double frequency followed by a digital frequency divider based on flip-flops. In this case, the portions of the circuit working at the double frequency could become a speed or power bottleneck.
3) Two cross-coupled VCO's [3].
4) Active polyphase filters such as ring oscillator designs. For instance, in four-delay stage ring oscillators, taps at diametrically opposite points yield quadrature phases [4].

In this work, we present an alternative method to obtain quadrature oscillators based on the differential coupling at the second harmonics of two differential oscillators. In fact, if there is phase shift of 180 degrees between the second harmonics of two oscillators, their fundamental frequency components will be in quadrature states.

To analyze the proposed design, two concepts related to oscillators should be revised: injected (or forced) and coupled oscillators. This is done in Section II and III, and the measurements are presented in Section IV.

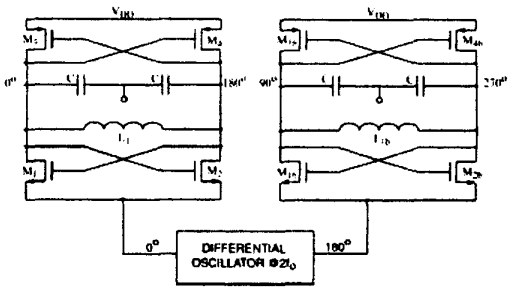

Fig. 1. Quadrature oscillator based on the injection of a differential second harmonic signal at the common-emitter nodes.

II. Super-Harmonic Injected Oscillators

In real oscillators, higher order harmonics, attenuated by the resonator tank, appear along with the fundamental frequency. For the differential configurations, it is even possible to find common-mode nodes where just even harmonics (mainly the second one) are present. Rategh and Lee have shown that, in differential oscillators, it is possible to use these common-mode nodes to inject a frequency close to twice the fundamental frequency of an oscillator and lock the oscillator to this injected signal [5]. As long as both oscillators keep locked, any change in the injected signal will be transmitted to the injected oscillator at the fundamental frequency. From this point of view, the oscillator is working as an analog frequency divider if we consider the fundamental harmonic as the circuit output. As a consequence, if two oscillators are

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injected by two-second harmonics with a phase shift of 180 degrees, their fundamental output will be in quadrature (Fig.1).

III. CIRCUIT TOPOLOGY

A simplified schematic of the quadrature oscillator is shown in Fig. 2. It consists of two complementary cross-pair CMOS oscillators coupled through an integrated transformer. The transformer is connected between the common-mode nodes at the sources of NMOS transistors and ground and substitutes the injection oscillator at $2f_o$ shown in Fig. 1. This transformer plays a fundamental role because it forces the required phase-shift of 180 degrees between the second harmonics present at the sources of NMOS transistors.

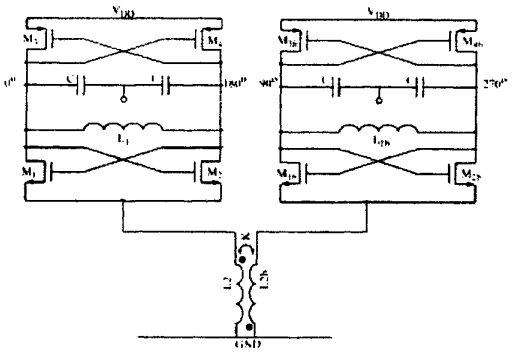

Fig. 2. Quadrature oscillator based on the differential coupling of the second harmonic through a planar inverting transformer.

The dynamics associated to coupled oscillators is inherently non-linear and has a rich set of possible states, ranging from the chaotic behavior to the mutual synchronization or locking. The ability of coupled oscillators to synchronize depends critically on the coupling network and the tendency to lock increases with increased coupling strength [6,7]. In our circuit, the transformer establishes a strong coupling between both oscillators so they can be seen as mutual injection-locked oscillators. As a consequence, both oscillators will be synchronized at the same frequency even if some mismatch exists between the resonant frequencies of the independent resonant tanks.

It has been shown that the possible states for coupled oscillators are finite. In particular, the on-phase-state with both signals in phase and the off-phase-state with signals shifted 180 degrees are natural configurations for coupled oscillators. Since we are interested in forcing the off-phase-state, a transformer in an inverter configuration has been used to couple both oscillators. A transformer in a non-inverting configuration will result in the oscillators coupled in the on-phase-state, and in-phase outputs at the fundamental frequency.

Moreover, any parasitic coupling at the fundamental frequency should be avoided since it could force the on-phase-state (or off-phase-state) between the two oscillators at the fundamental frequency. This coupling could be through the silicon substrate or via magnetic coupling of the inductors of the resonant tanks. Electromagnetic simulations of closely-spaced inductors have been carried out using Momemtum (Agilent Technologies) to analyze the magnetic coupling between two planar inductors. Results show that for the inductor spacing used in our layout, 250 μm, the coupling is lower than -25 dB and has negligible effects on the design. Another problem is that the fundamental frequency could appear on the transformer terminals (on the emitters) as a consequence of transistor mismatches. However, this effect has been simulated and can be reasonably neglected.

IV. CIRCUIT DESIGN

The quadrature oscillator was implemented in the Conexant 0.35 μm BiCMOS process [8]. The standard complementary CMOS cross-pair topology has been used since the structure combining PMOS and NMOS cross-pairs achieves a lower phase noise than a single NMOS topology for the same power due to symmetry properties of the resulting periodic waveform [9]. Also, the current source typically found at the sources of NMOS transistors has been substituted by the planar transformer. Omitting the current source reduces the voltage required by the oscillator and removes an important noise source at the expense of an increased sensitivity to power supply changes (frequency pushing). In the future, it is straightforward to include a current source in series with the transformer or connected at the sources of the PMOS transistors.

Spectre RF (Cadence) simulation was used during the design process in order to obtain optimum sizes and bias conditions for minimum phase noise. Transistors with minimum channel length (i.e, 0.35 μm) were used to minimize the parasitic capacitances. The transistor W/L ratios were chosen for minimum phase noise as long as a reliable startup of the oscillator was guaranteed for a voltage supply of 1.8 V. Two common-drain differential amplifier stages, biased at 5 mA per stage, and each adding around 50 fF to the resonant tanks, were used as output buffers to drive the 50 Ω measurement system.

During the layout process, special care was taken to keep the inherent symmetry of the circuit. Both NMOS and PMOS transistors were layed out as multi-finger structures in order to minimize the gate resistance.

The integrated transformer used consists of two closely-coupled loops of six turns with a metal width of 8 μm, a turn-to-turn spacing of 2 μm and an outer dimension of 250 μm (Fig. 3) resulting in a coupling factor of 0.83. It was implemented using the top metal with a sheet resistivity of 10 mΩ/sq, and is separated by a silicon-dioxide dielectric layer of 3 μm from a 10 Ω-cm silicon substrate. The design results in a Q of 9 at 1.8 GHz.

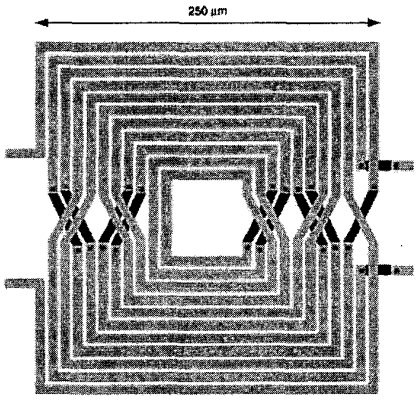

Fig. 3. The integrated transformer with a simulated Q of 9 at 1.8 GHz.

Obviously, the transformer characteristics play an important role in the proposed circuit and in particular the coupling factor and the phase shift between primary and secondary loops. As a consequence, an accurate and optimized design of this component is required. This is currently being done and will be presented at the conference.

V. MEASUREMENTS

The VCO core consumes 3 mA (both oscillators) from a 1.7 V supply. The chip dimensions, 1250 x 1250 μm, were defined by the size of the differential probes available for on-wafer test. The outputs were measured using a differential probe (G-S-G-S-G) from Picoprobe and converted to single-ended signal using a 0-180° power-combiner. The measured output power -9 dBm per oscillator at 900 MHz.

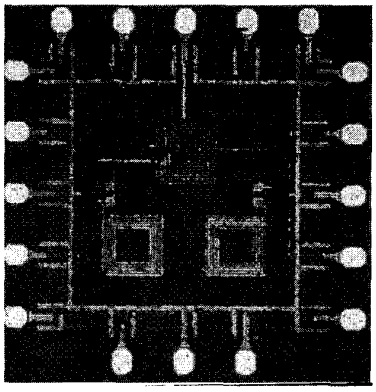

Fig.4. Photomicrograph of the 900 MHz quadrature CMOS oscillator. The inverting transformer is placed between the differential oscillators. Chip dimensions: 1.25x1.25 mm.

The VCO phase-noise was measured in Agere Systems using the Agilent E5500 phase noise measurement system with the FM discrimination method. The phase noise results in −116, −133 and −138 dBc/Hz at 100 KHz, 600 KHz and 1 MHz from the carrier, respectively. The delay line used introduced 27 ns of delay, establishing a trade-off between the noise floor and the maximum offset frequency measurable accurately. The results are shown in Fig. 5.

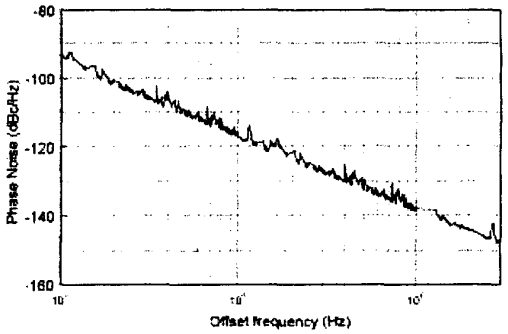

Fig. 5. Measured phase-noise of the integrated CMOS quadrature oscillator at 900 MHz.

The time domain outputs were measured using a 26 Gsamples oscilloscope in order to observe the quadrature conditions. The setup used to realize the quadrature measurement, shown in Fig. 6, includes 180-deg. couplers, power splitters and cables, and could not be perfectly matched. Therefore, some departure from the

quadrature should be associated to the measurement setup. The overall losses of this path were around 5 dB (4.3 dB due to the power splitter used to generate the trigger signal). The real amplitudes of the signals are therefore around 125 mV at 900 MHz (-9 dBm).

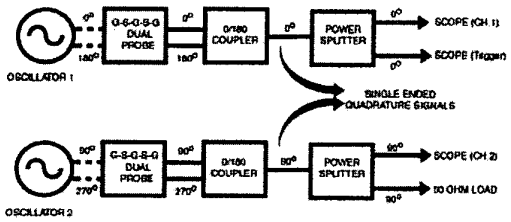

Fig. 6. Setup for the measurement of the quadrature signals in the time domain.

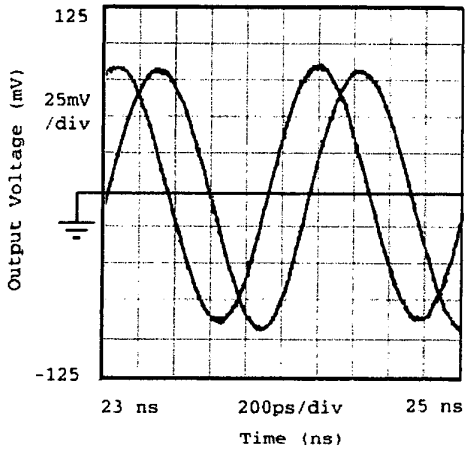

Fig. 7. Measured time-domain outputs of the quadrature oscillator.

VI. Conclusion

In this work, a novel method to obtain quadrature oscillators based on the differential coupling at the second harmonic frequency of two differential oscillators is presented. An integrated quadrature CMOS oscillator at 900 MHz with a differential output power of –9 dBm has been presented. The power consumption of the oscillator core is 5 mW and results in a phase-noise of -116, -133 and –138 dBc/Hz at 100 KHz, 600 KHz and 1 MHz from the carrier, respectively.

The proposed design method is applicable to other any differential topologies, such as the Colpitts oscillator, or the cross-coupled BJT or SiGe oscillator. Also, this method is especially applicable at 2.5-5 GHz and above where the power associated with building a 5-10 GHz differential oscillator followed by a digital divider becomes too high.

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References

[1] Abidi, A.A., " Direct-conversion radio transceivers for digital communications", *Solid-State Circuits, IEEE Journal of*, Volume: 30 Issue: 12, pp. 1399 –1410, Dec. 1995.

[2] Craninckx, J.; Steyaert, M.S.J. " A fully integrated CMOS DCS-1800 frequency synthesizer", *Solid-State Circuits, IEEE Journal of*, Volume: 33 Issue: 12, pp. 2054 –2065.Dec. 1998

[3] Rofougaran, A.; Rael, J.; Rofougaran, M.; Abidi, " A 900 MHz CMOS LC-oscillator with quadrature outputs," *Solid-State Circuits Conference, 1996. Digest of Technical Papers.* 42nd ISSCC., pp. 392 –393 , 1996 IEEE International , 1996

[4] Vancorenland, P.; Steyaert, M. " A 1.57 GHz fully integrated very low phase noise quadrature VCO," *VLSI Circuits, 2001. Digest of Technical Papers.* 2001 Symposium on, pp. 111 –114, 2001

[5] Rategh, H.R.; Lee, T.H. " Superharmonic injection-locked frequency dividers," *Solid-State Circuits, IEEE Journal of*, Volume: 34 Issue: 6, pp. 813 –821, June 1999

[6] Lynch, J.J.; York, R.A. " Synchronization of oscillators coupled through narrow-band networks," *Microwave Theory and Techniques, IEEE Transactions on*, Volume: 49 Issue: 2, pp. 237 –249, Feb. 2001

[7] Ram, R.J.; Sporer, R.; Blank, H-R.; York, R.A. . " Chaotic dynamics in coupled microwave oscillators," *Microwave Theory and Techniques, IEEE Transactions on*, Volume: 48 Issue: 11 Part: 1, pp. 1909 –1916, Nov. 2000

[8] M. Casanelli et al. "BC35: a 0.35 μm, 30 GHz, Production RF BiCMOS Technology", *IEEE BCTM*, 1999, pp.125-129

[9] *Hajimiri, A.; Lee, T.H.* "Design issues in CMOS differential LC oscillators" *Solid-State Circuits, IEEE Journal of*, Volume: 34 Issue: 5, pp. 717 –724, May 1999